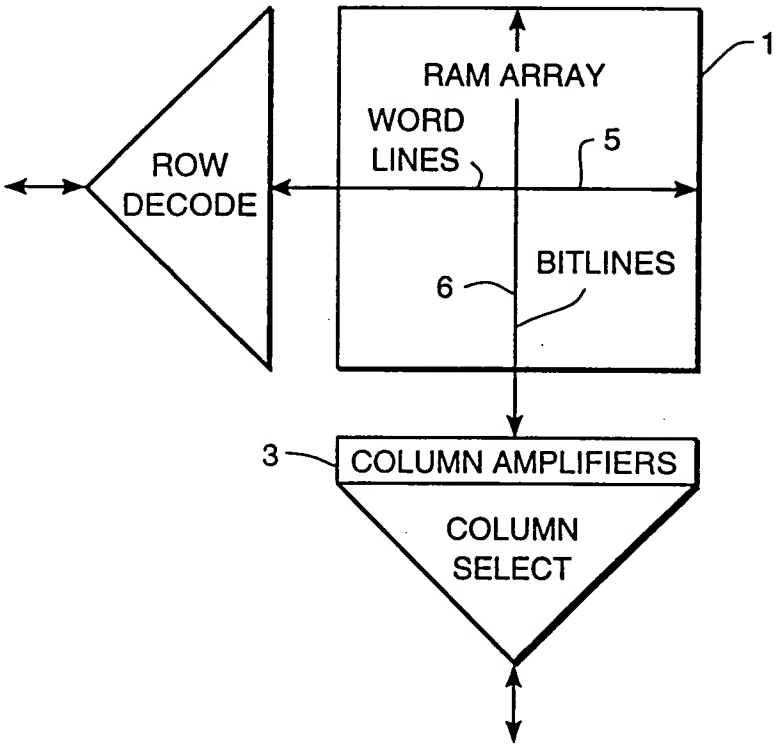
FIG_1


RAM ARRAY
1
WORD
LINES
5
ROW
DECODE
BITLINES
6
3
COLUMN AMPLIFIERS
COLUMN
SELECT

08820 EP 0 628 918 A1

FIG_2

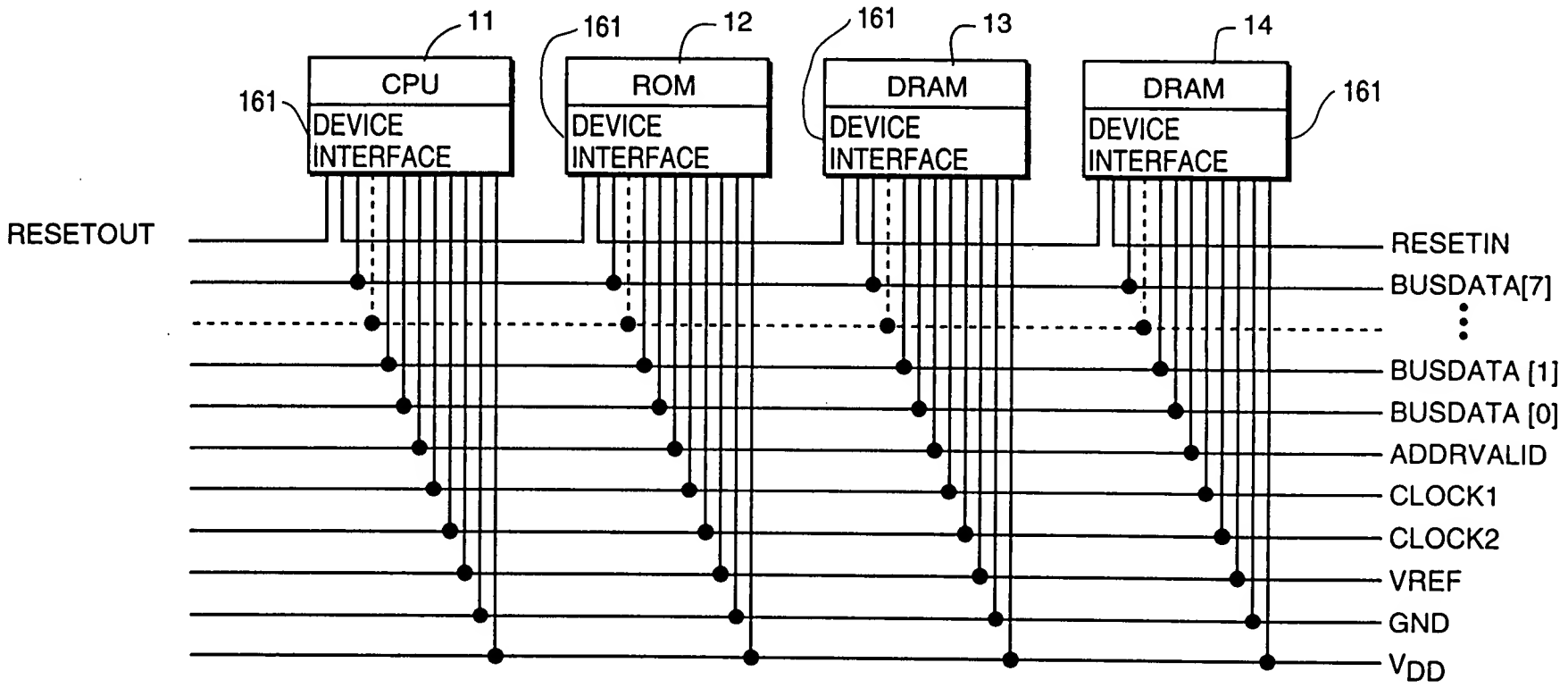
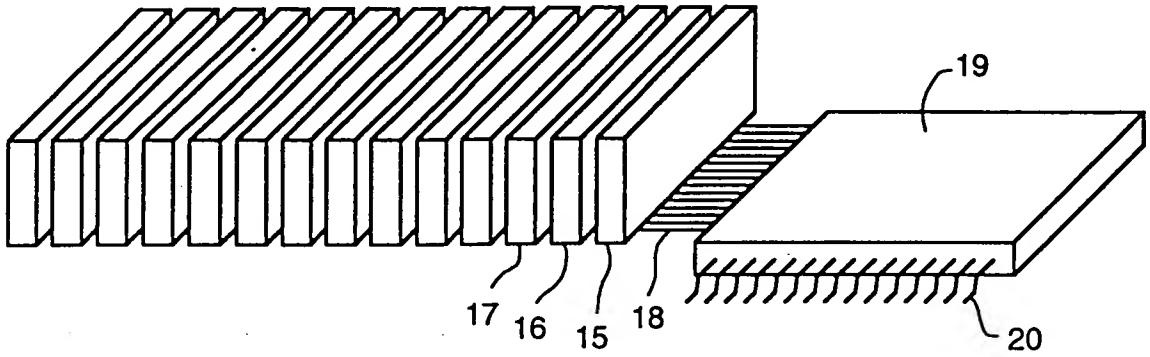


FIG_3



REGULAR ACCESS

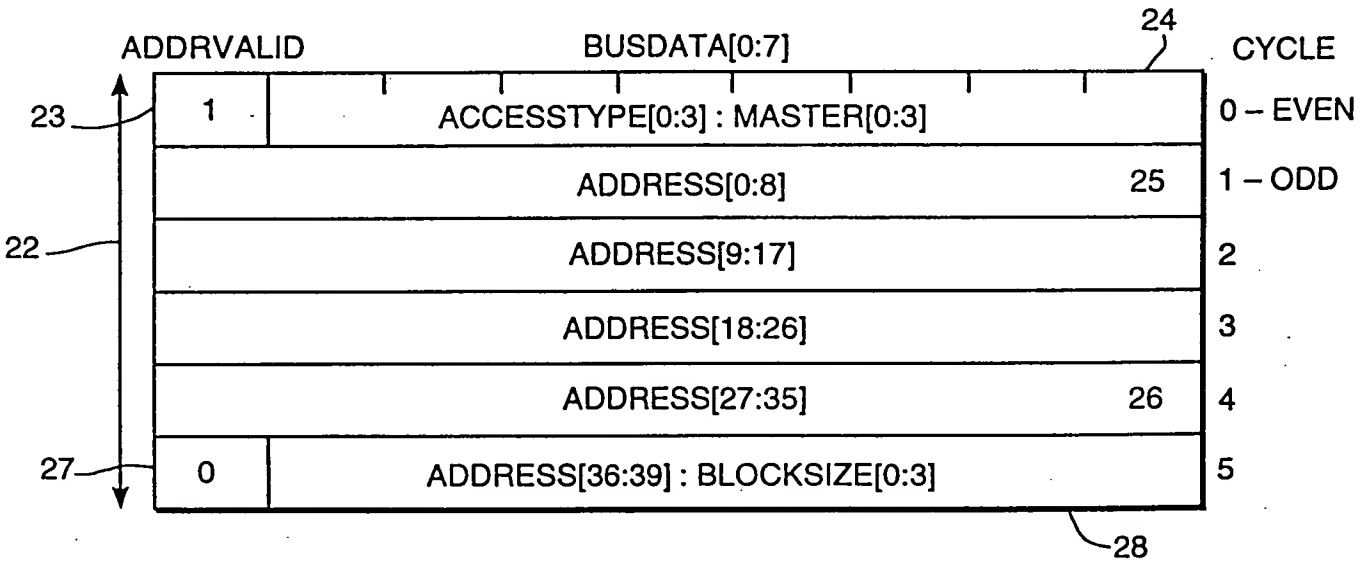


FIG_4

REJECT (NACK) CONTROL PACKET

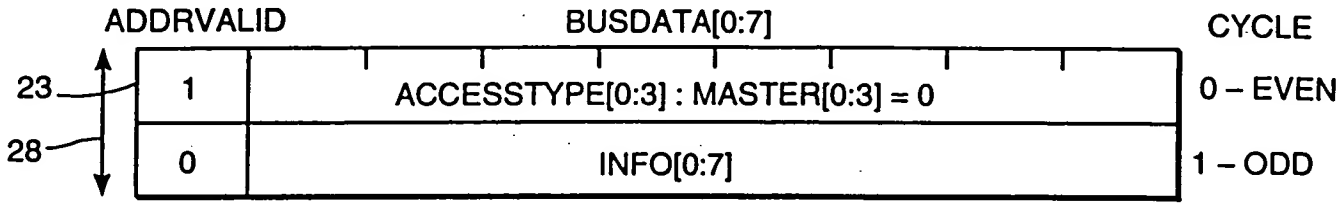


FIG_5

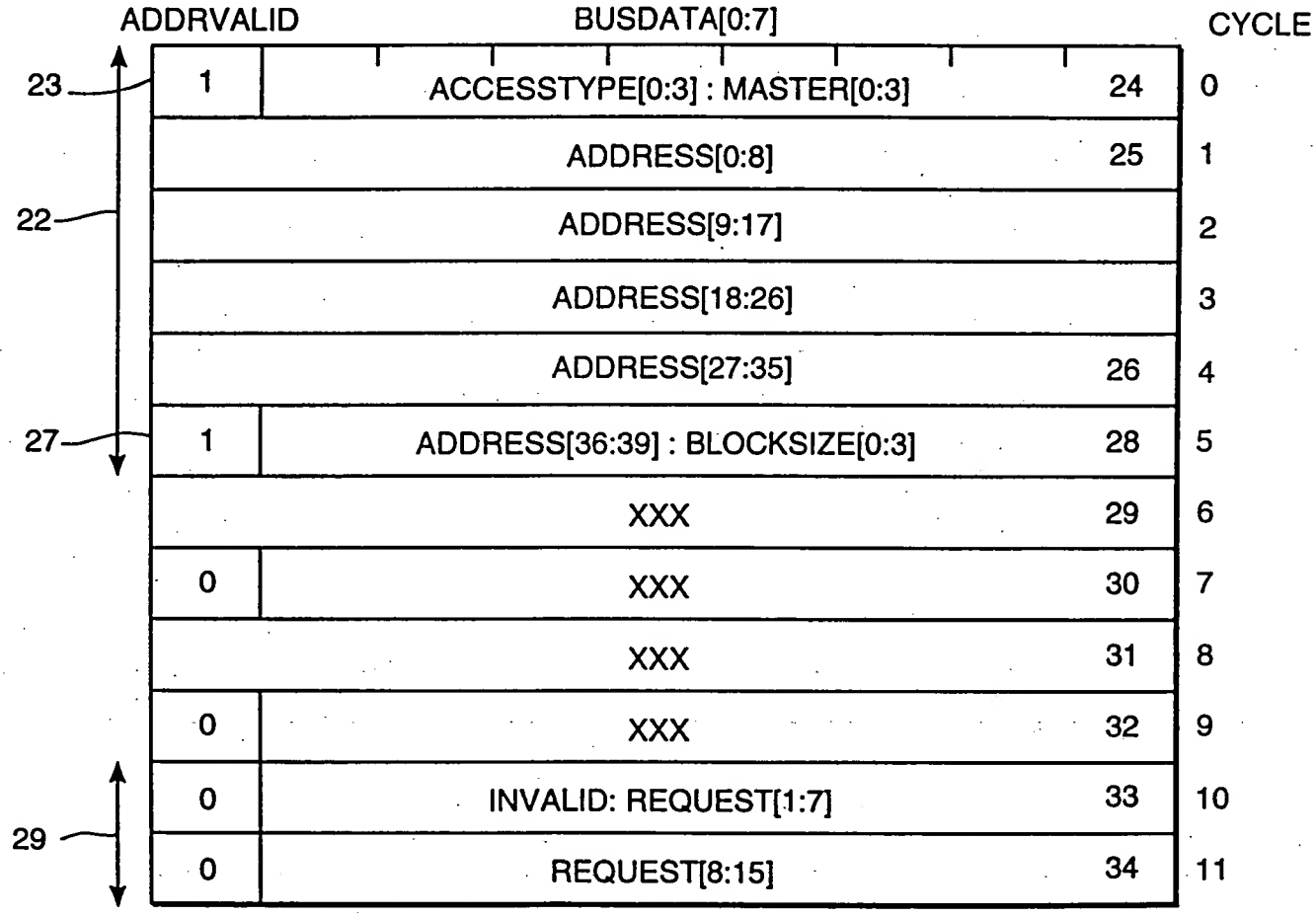


FIG_6

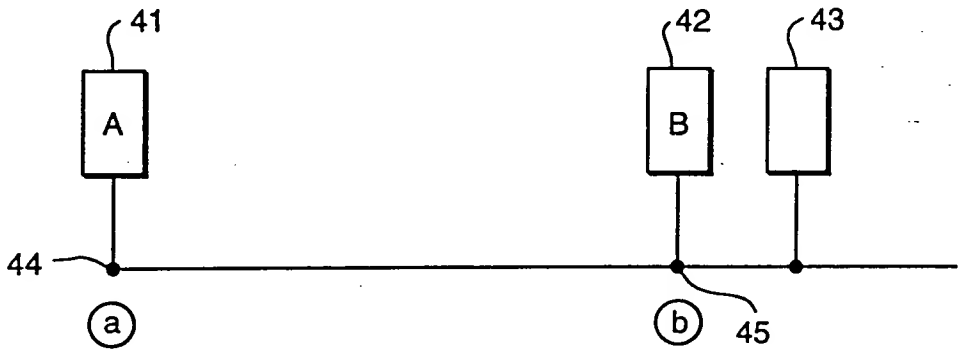


FIG_7A

DO8201 E2811560

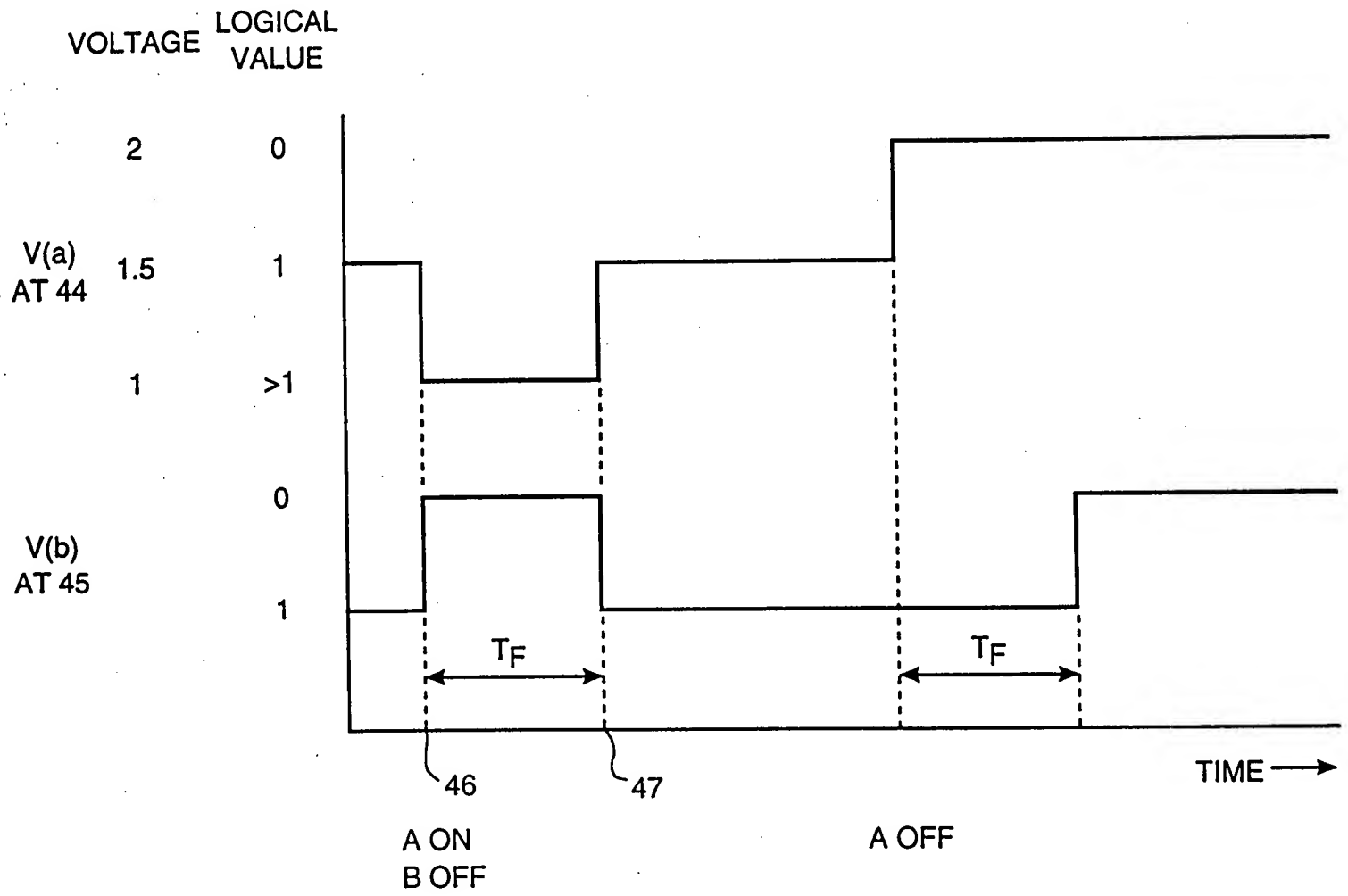


FIG_7B

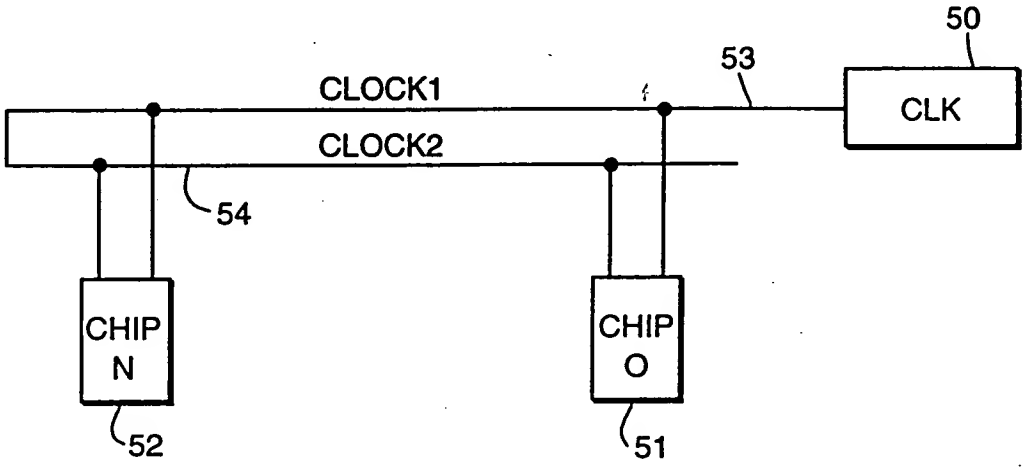

50
53
CLOCK1
CLK
CLOCK2
54
CHIP N
CHIP O
52
51

FIG_8A

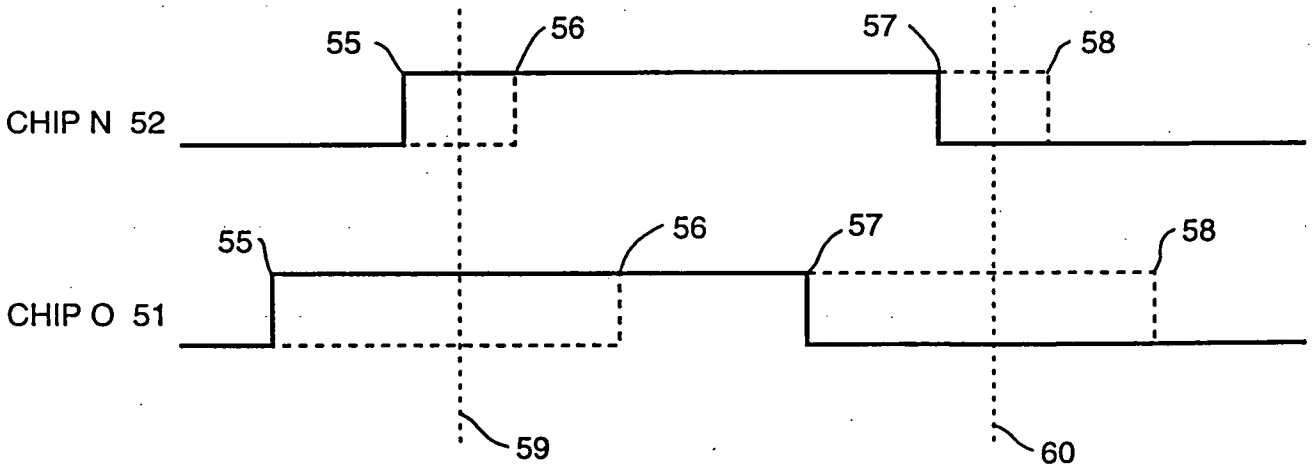
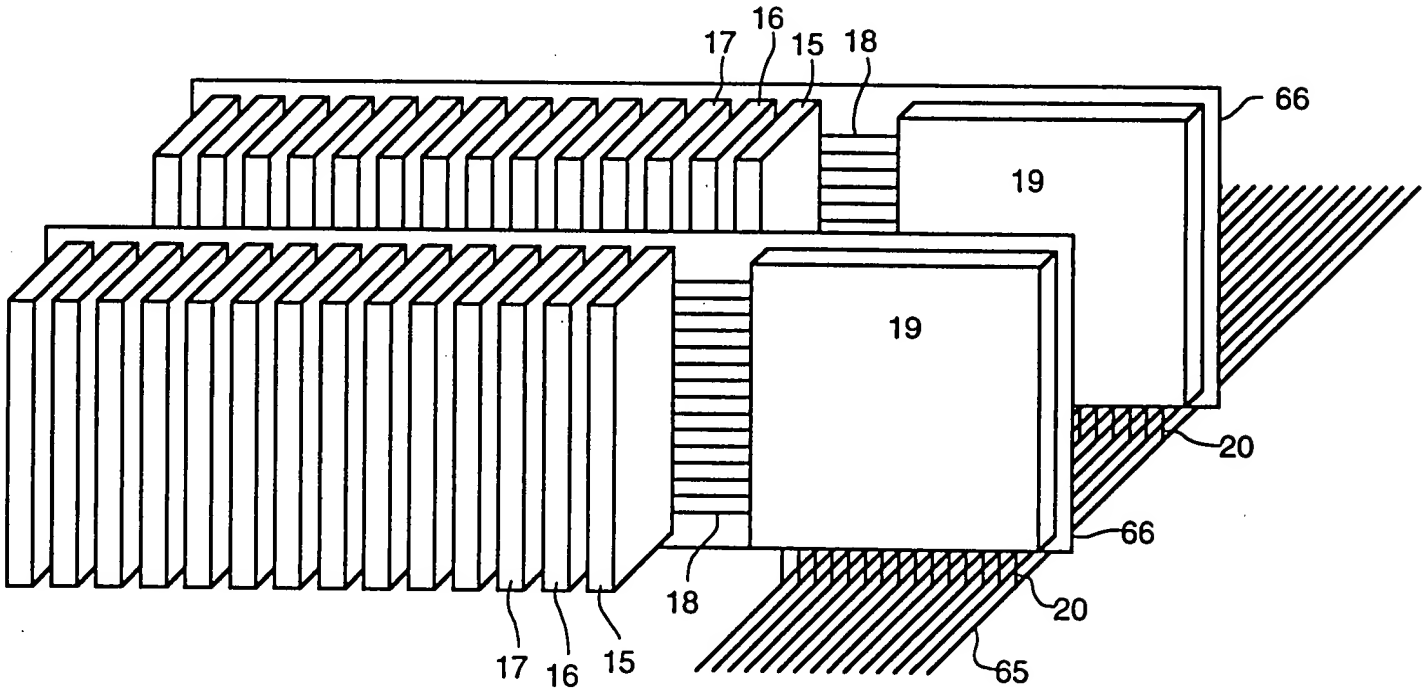

55
56
57
58
CHIP N 52
55
56
57
58
CHIP O 51
59
60

FIG_8B

0082807 2281360

FIG_9



08820 2281560

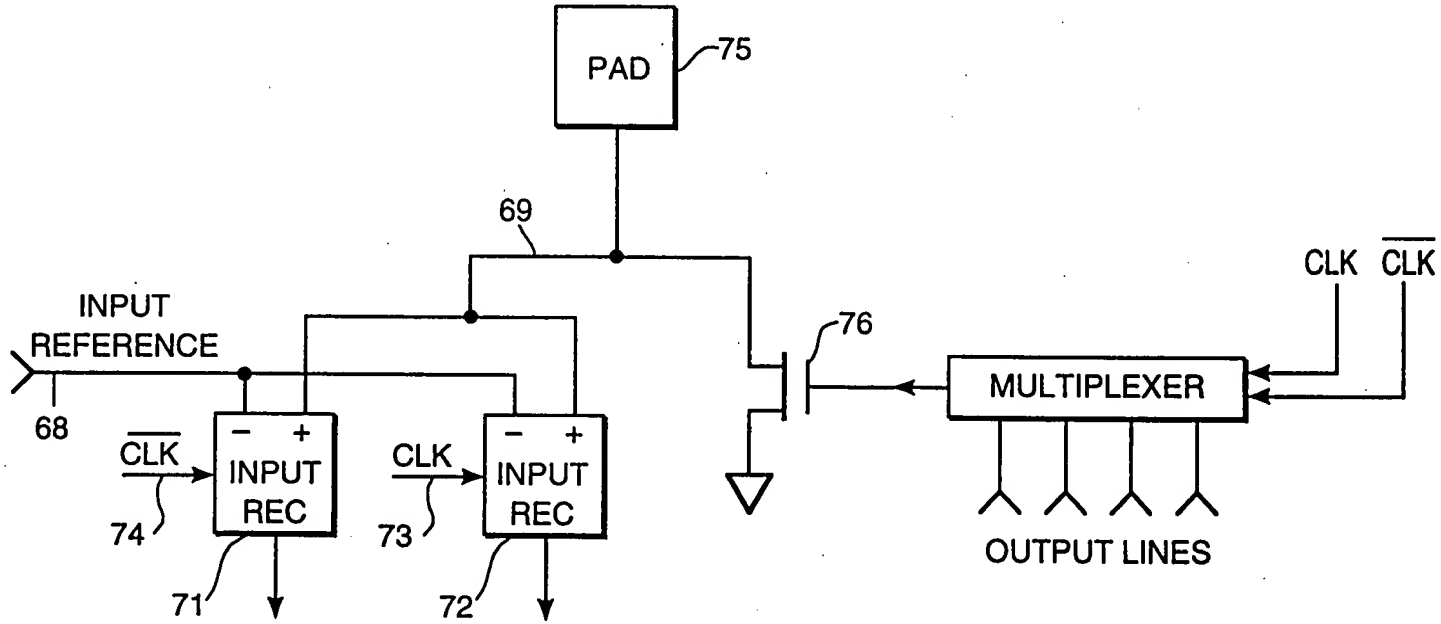
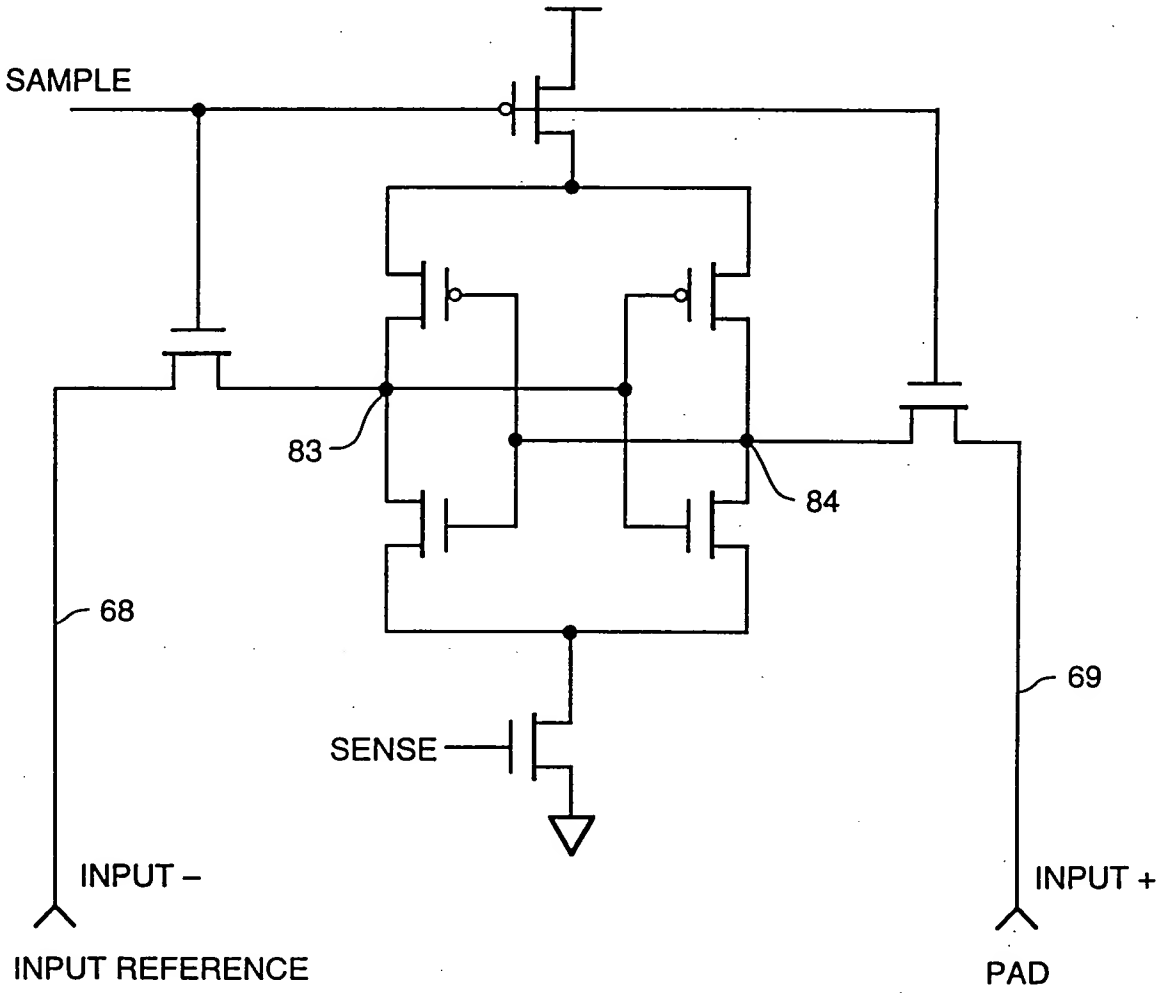


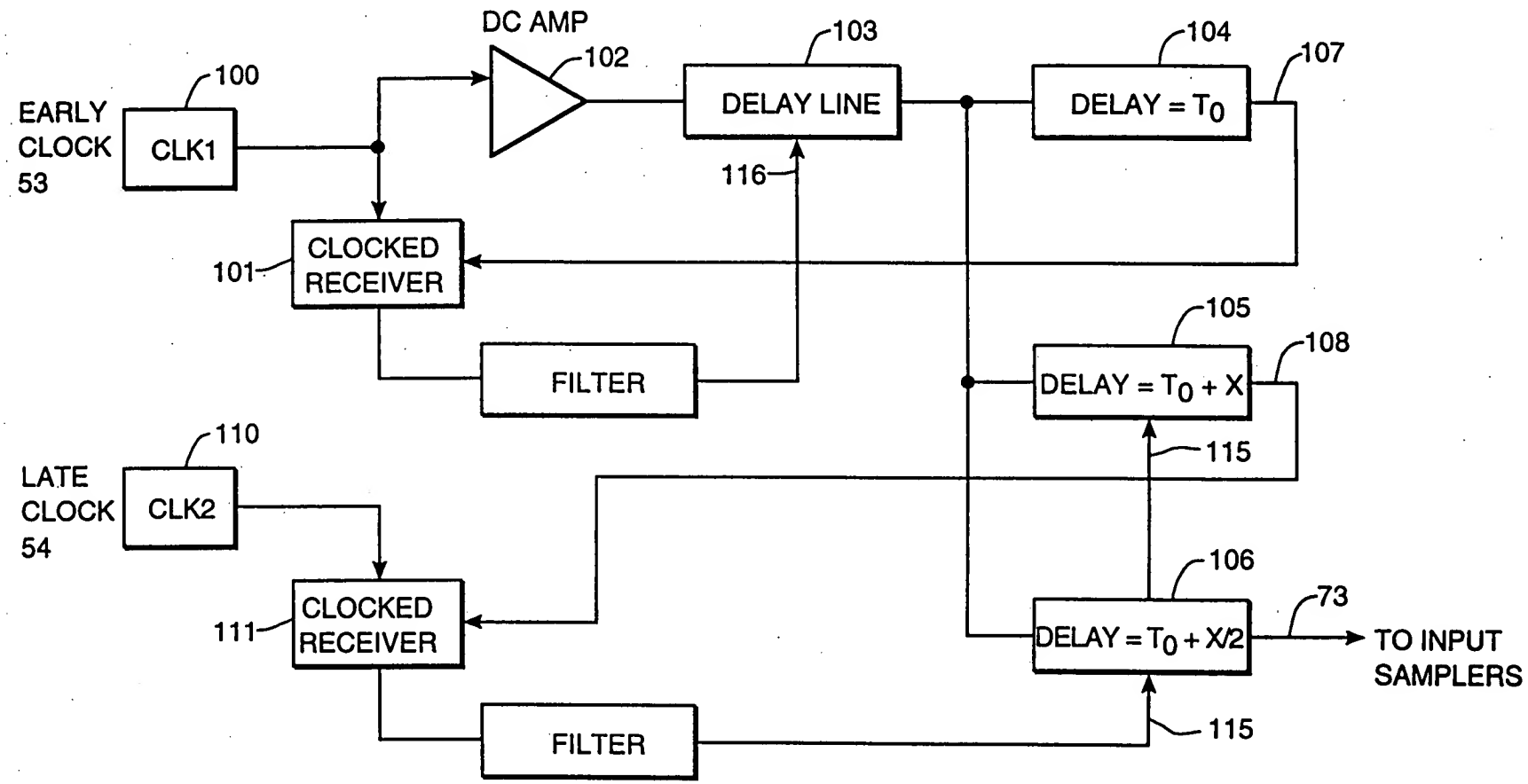
FIG_10

FIG_11



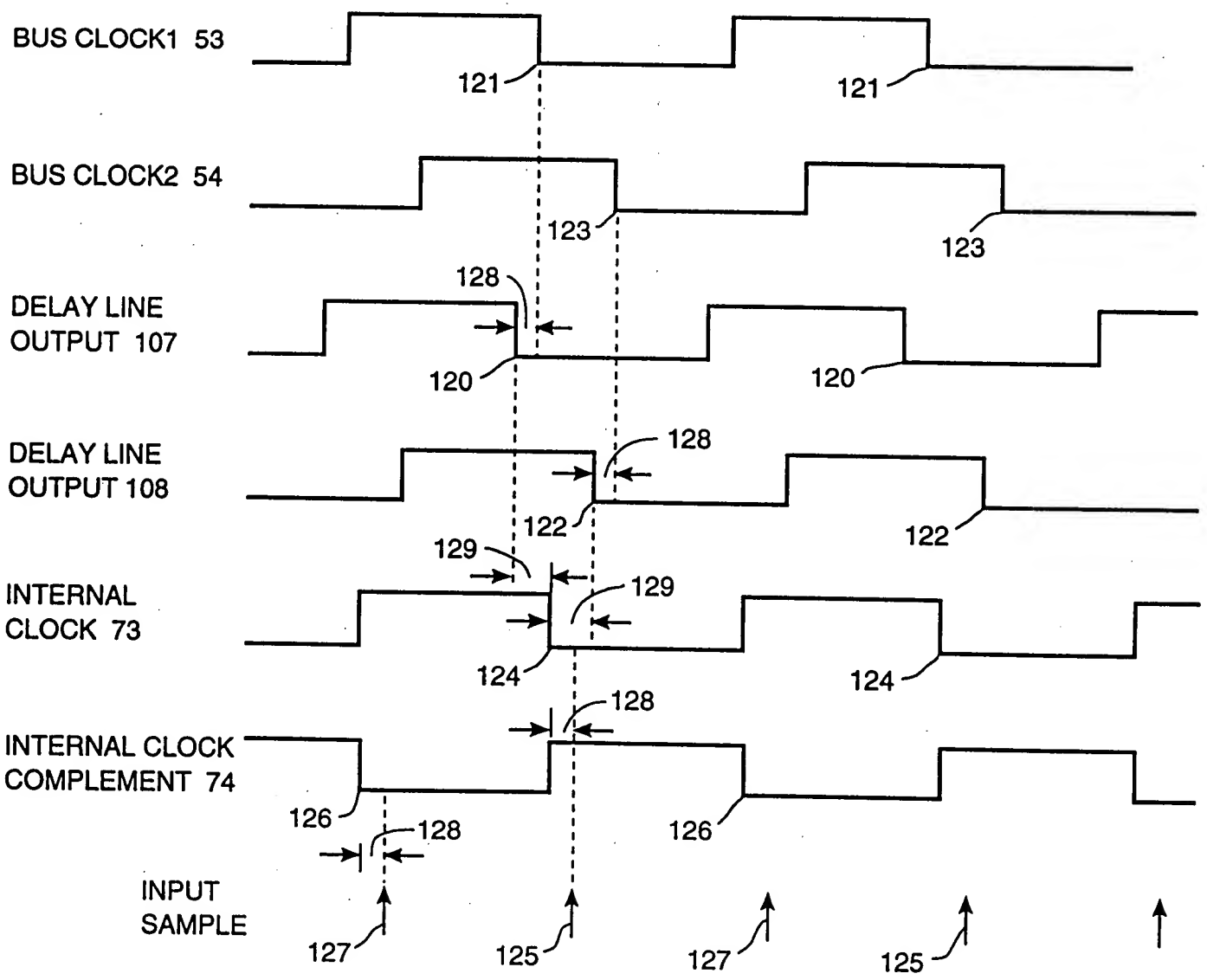
08820 "28TS60

FIG_12



6083201 2284560

FIG_13



D08220 "2681560

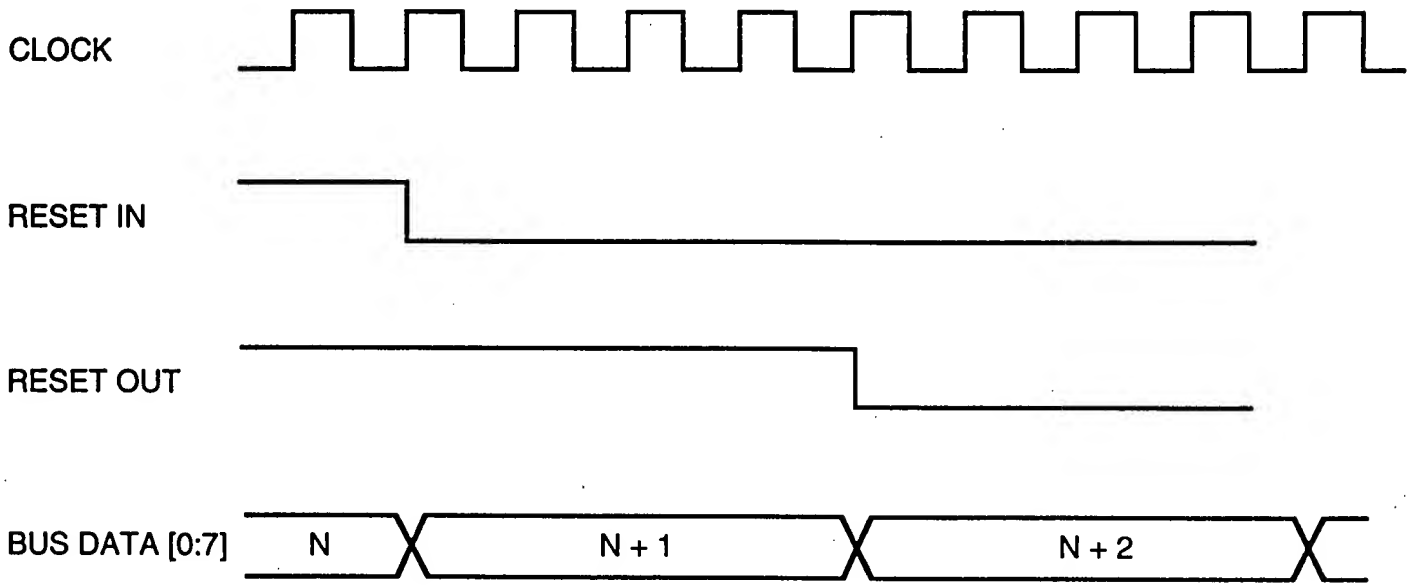
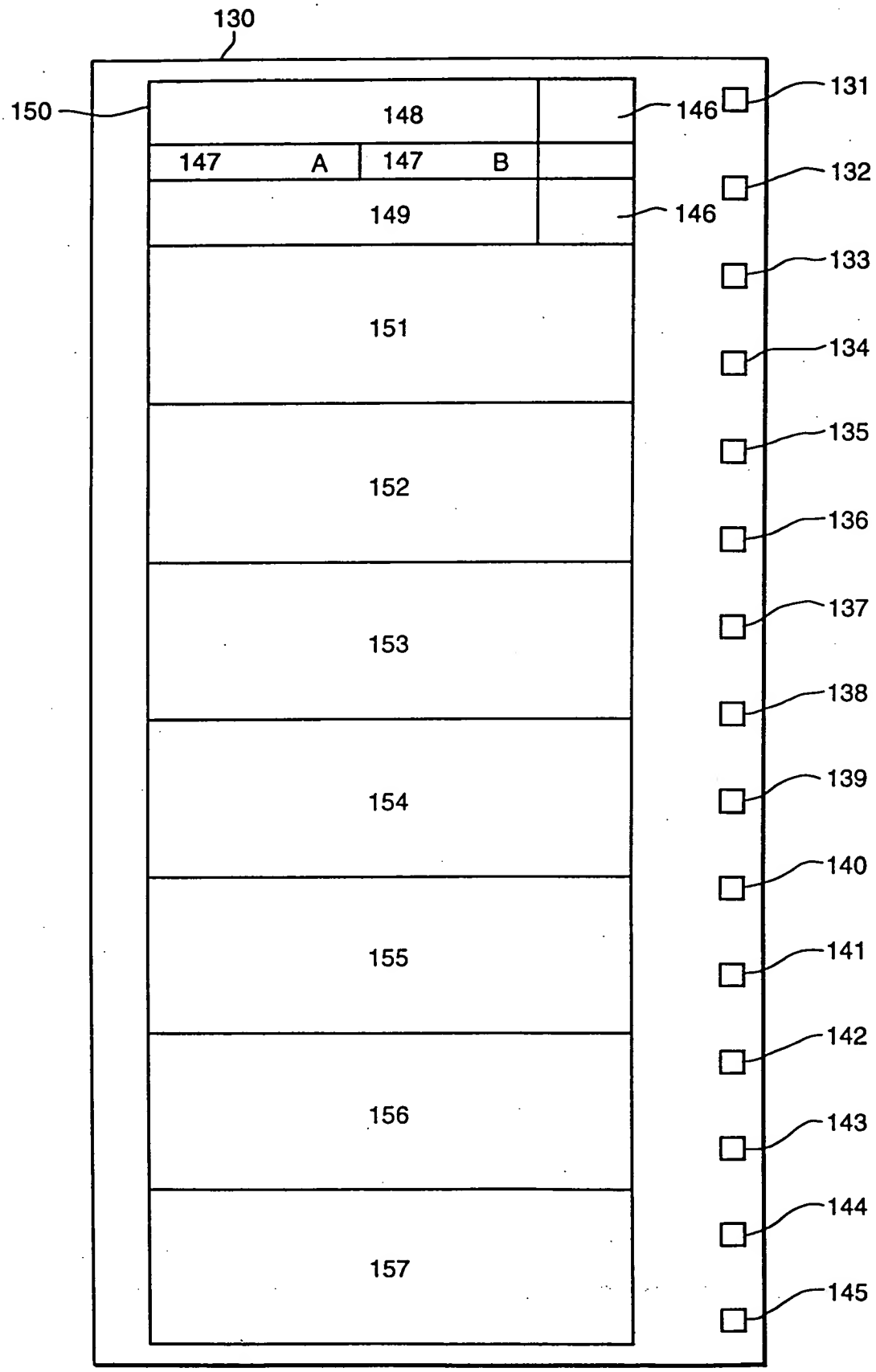


FIG_14

FIG_15


130
150
148
146
131
147
A
147
B
132
149
146
133
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145

DO8220 28bit560

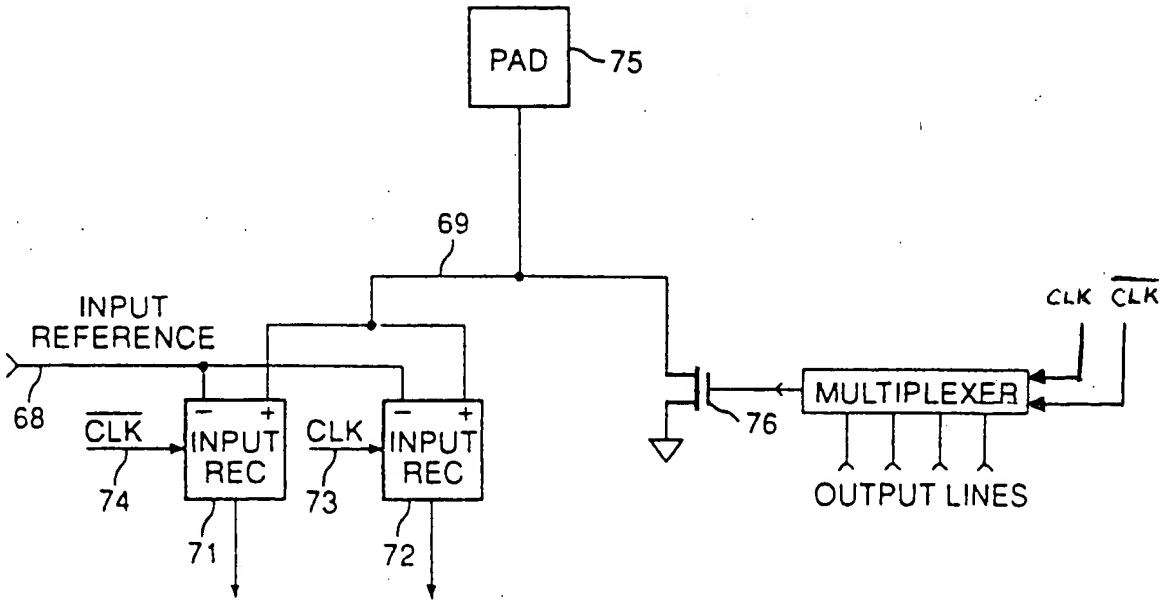

FIG. 10

08820.2681560

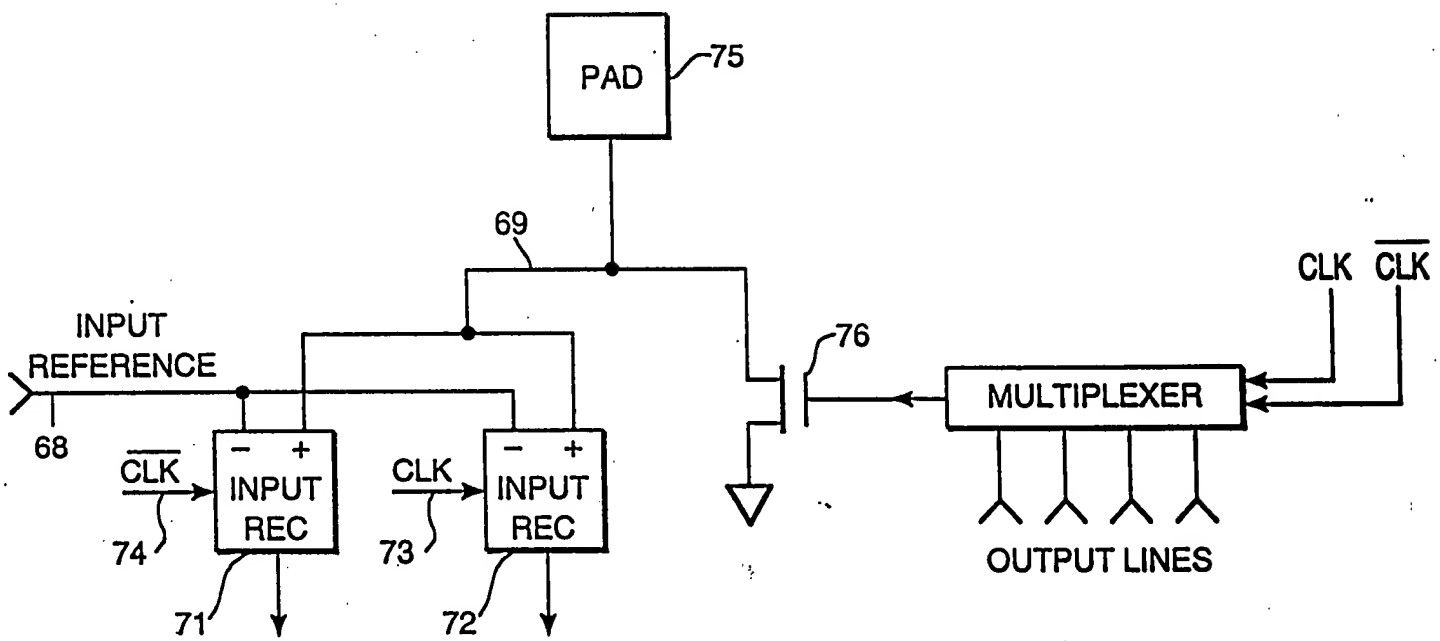

FIG_10